

MC1741C

Internally Compensated, High Performance Operational Amplifier

The MC1741C was designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

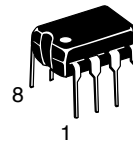
- No Frequency Compensation Required
- Short Circuit Protection
- Offset Voltage Null Capability
- Wide Common Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch Up



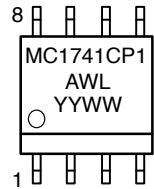
ON Semiconductor

<http://onsemi.com>

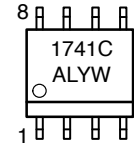
MARKING DIAGRAMS



PDIP-8
P1 SUFFIX
CASE 626

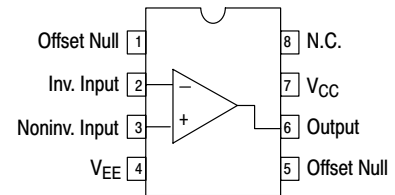


SO-8
D SUFFIX
CASE 751



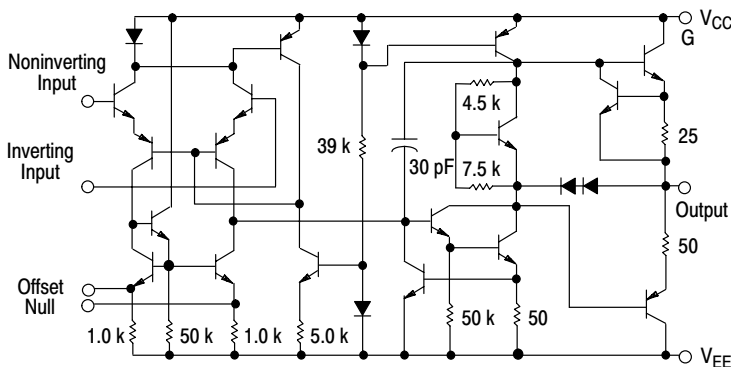
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS



(Top View)

Equivalent Circuit Schematic (1/4 of Circuit Shown)



ORDERING INFORMATION

| Device | Package | Shipping |
|------------|---------|------------------|
| MC1741CD | SO-8 | 98 Units/Rail |
| MC1741CDR2 | SO-8 | 2500 Tape & Reel |
| MC1741CP1 | PDIP-8 | 50 Units/Rail |

MC1741C

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|------------------|-------------|------|
| Power Supply Voltage | V_{CC}, V_{EE} | ± 18 | Vdc |
| Input Differential Voltage | V_{ID} | ± 30 | V |
| Input Common Mode Voltage (Note 1.) | V_{ICM} | ± 15 | V |
| Output Short Circuit Duration (Note 2.) | t_{SC} | Continuous | – |
| Operating Ambient Temperature Range | T_A | 0 to +70 | °C |
| Storage Temperature Range | T_{stg} | –55 to +125 | °C |

- For supply voltages less than +15 V, the absolute maximum input voltage is equal to the supply voltage.
- Supply voltage equal to or less than 15 V.

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15$ V, $V_{EE} = -15$ V, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|-----------|----------------------|----------------------|--------|------------------|
| Input Offset Voltage ($R_S \leq 10$ k) | V_{IO} | – | 2.0 | 6.0 | mV |
| Input Offset Current | I_{IO} | – | 20 | 200 | nA |
| Input Bias Current | I_{IB} | – | 80 | 500 | nA |
| Input Resistance | r_i | 0.3 | 2.0 | – | M Ω |
| Input Capacitance | C_i | – | 1.4 | – | pF |
| Offset Voltage Adjustment Range | V_{IOR} | – | ± 15 | – | mV |
| Common Mode Input Voltage Range | V_{ICR} | ± 12 | ± 13 | – | V |
| Large Signal Voltage Gain ($V_O = \pm 10$ V, $R_L \geq 2.0$ k) | A_{VOL} | 20 | 200 | – | V/mV |
| Output Resistance | r_o | – | 75 | – | Ω |
| Common Mode Rejection ($R_S \leq 10$ k) | CMR | 70 | 90 | – | dB |
| Supply Voltage Rejection ($R_S \leq 10$ k) | PSR | 75 | – | – | dB |
| Output Voltage Swing ($R_L \geq 10$ k) ($R_L \geq 2.0$ k) | V_O | ± 12 ± 10 | ± 14 ± 13 | – – | V |
| Output Short Circuit Current | I_{SC} | – | 20 | – | mA |
| Supply Current | I_D | – | 1.7 | 2.8 | mA |
| Power Consumption | P_C | – | 50 | 85 | mW |
| Transient Response (Unity Gain, Noninverting) ($V_i = 20$ mV, $R_L \geq 2.0$ k, $C_L \leq 100$ pF) Rise Time | t_{TLH} | – | 0.3 | – | μs |
| ($V_i = 20$ mV, $R_L \geq 2.0$ k, $C_L \leq 100$ pF) Overshoot | os | – | 15 | – | % |
| ($V_i = 10$ V, $R_L \geq 2.0$ k, $C_L \leq 100$ pF) Slew Rate | SR | – | 0.5 | – | V/ μs |

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15$ V, $V_{EE} = -15$ V, $T_A = T_{low}$ to T_{high} , unless otherwise noted.)*

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|-----------|----------|----------|-----|------|
| Input Offset Voltage ($R_S \leq 10$ k Ω) | V_{IO} | – | – | 7.5 | mV |
| Input Offset Current ($T_A = 0^\circ$ to $+70^\circ\text{C}$) | I_{IO} | – | – | 300 | nA |
| Input Bias Current ($T_A = 0^\circ$ to $+70^\circ\text{C}$) | I_{IB} | – | – | 800 | nA |
| Supply Voltage Rejection ($R_S \leq 10$ k) | PSR | 75 | – | – | dB |
| Output Voltage Swing ($R_L \geq 2.0$ k) | V_O | ± 10 | ± 13 | – | V |
| Large Signal Voltage Gain ($R_L \geq 2.0$ k, $V_O = \pm 10$ V) | A_{VOL} | 15 | – | – | V/mV |

* $T_{low} = 0^\circ\text{C}$ $T_{high} = 70^\circ\text{C}$

MC1741C

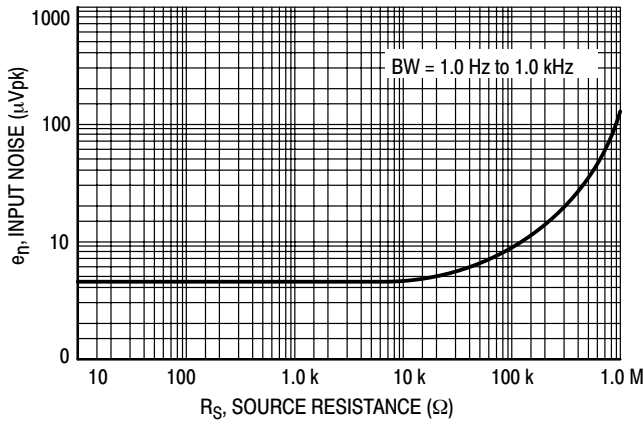


Figure 1. Burst Noise versus Source Resistance

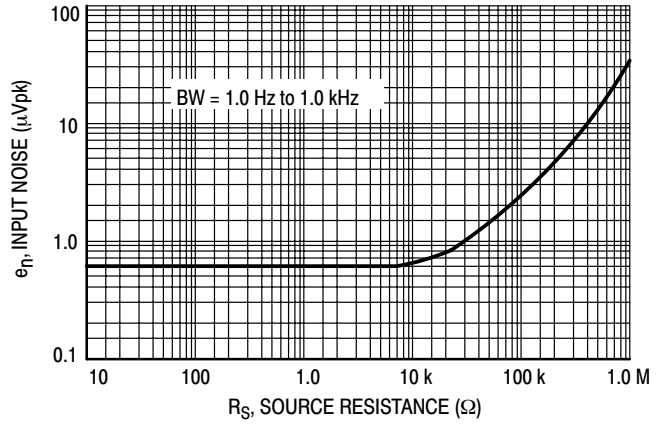


Figure 2. RMS Noise versus Source Resistance

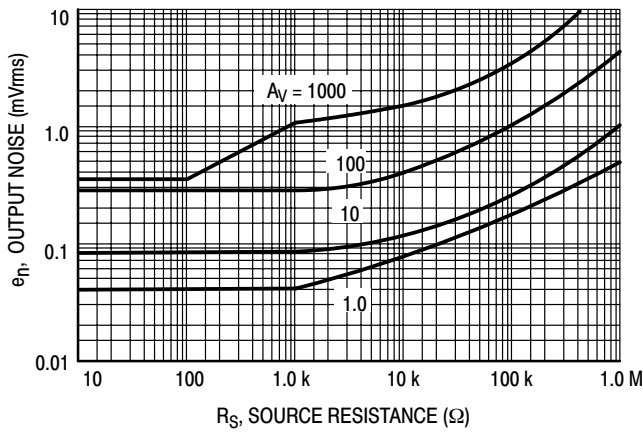


Figure 3. Output Noise versus Source Resistance

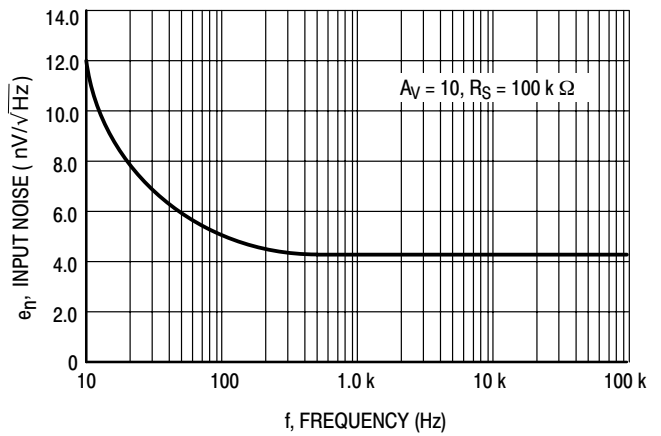
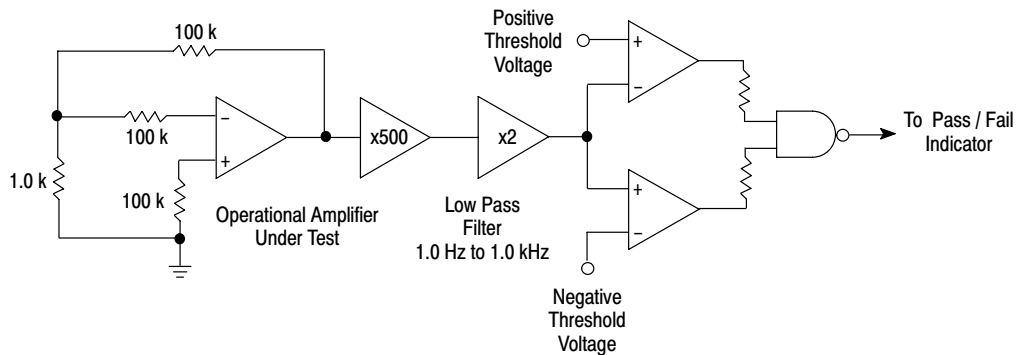


Figure 4. Spectral Noise Density



Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 sec and the 20 mV peak limit refers to the operational amplifier input thus eliminating errors in the closed loop gain factor of the operational amplifier.

Figure 5. Burst Noise Test Circuit

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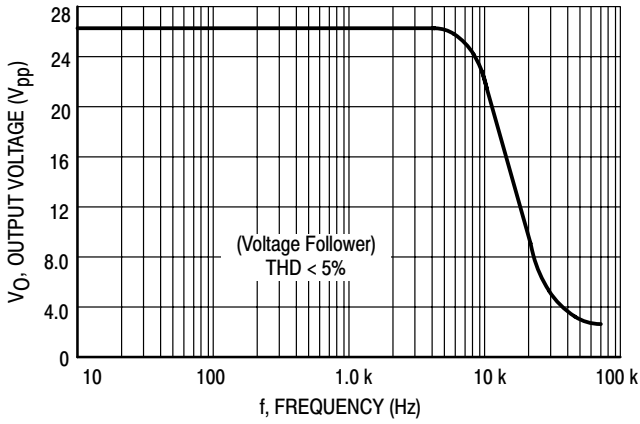


Figure 6. Power Bandwidth (Large Signal Swing versus Frequency)

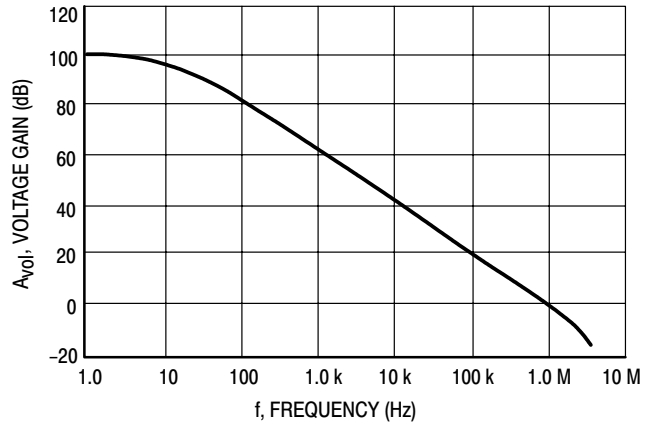


Figure 7. Open Loop Frequency Response

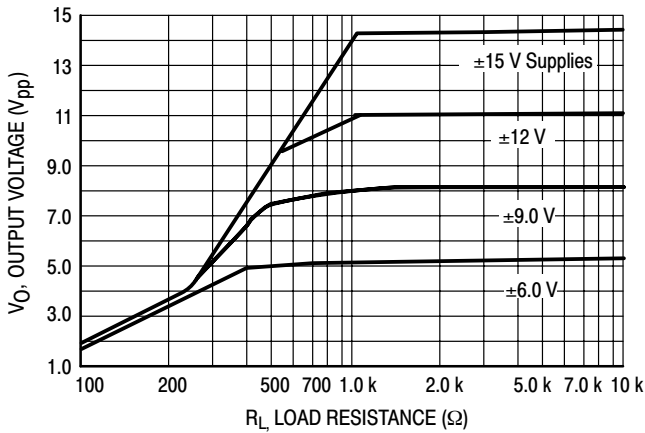


Figure 8. Positive Output Voltage Swing versus Load Resistance

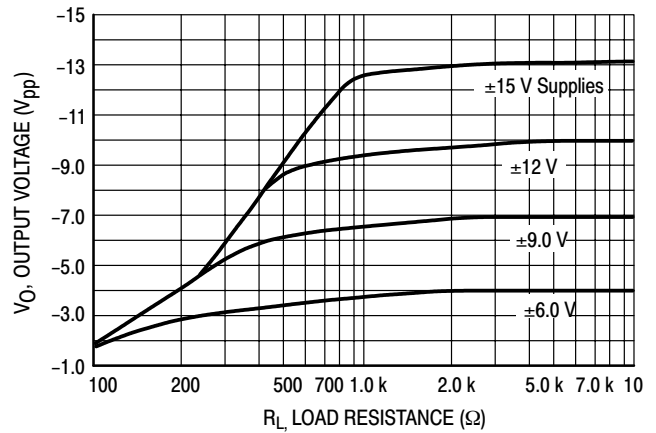


Figure 9. Negative Output Voltage Swing versus Load Resistance

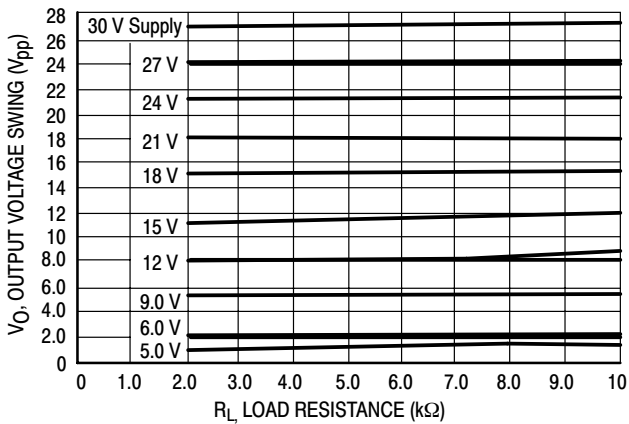


Figure 10. Output Voltage Swing versus Load Resistance (Single Supply Operation)

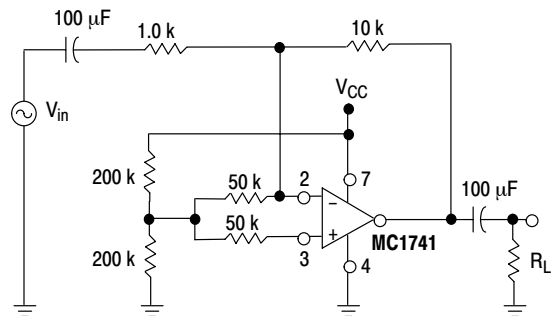


Figure 11. Single Supply Inverting Amplifier

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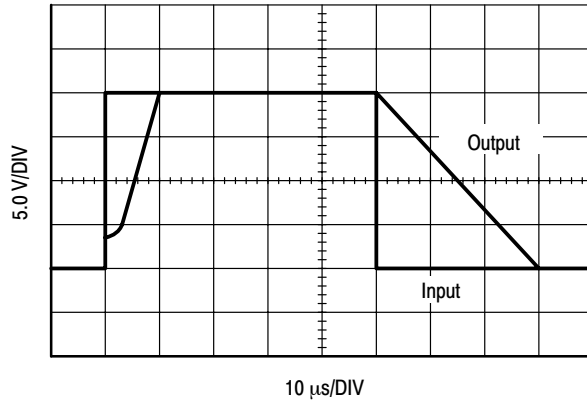


Figure 12. Noninverting Pulse Response

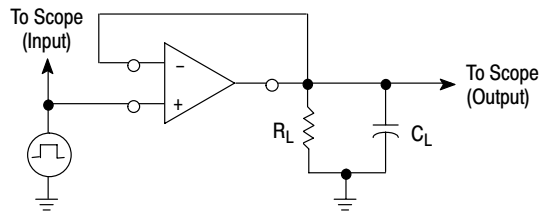


Figure 13. Transient Response Test Circuit

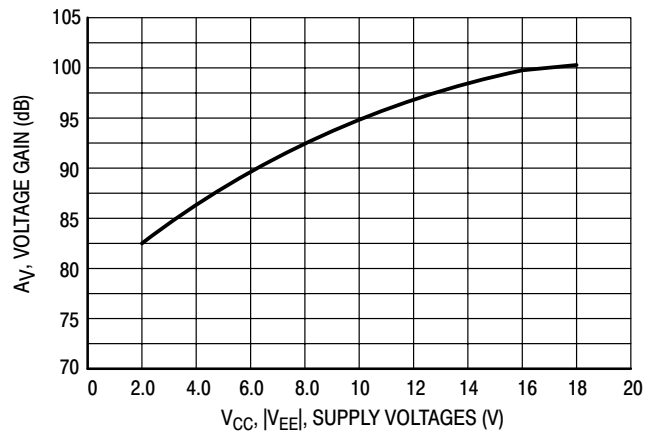
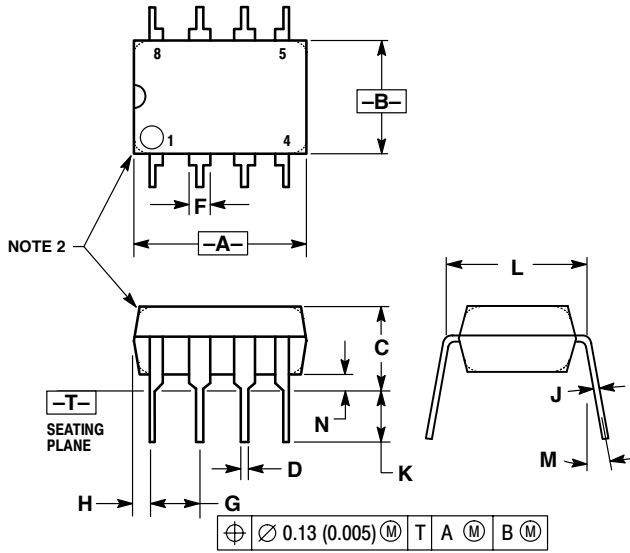


Figure 14. Open Loop Voltage Gain versus Supply Voltage

MC1741C

PACKAGE DIMENSIONS

PDIP-8
P1 SUFFIX
CASE 626-05
ISSUE K

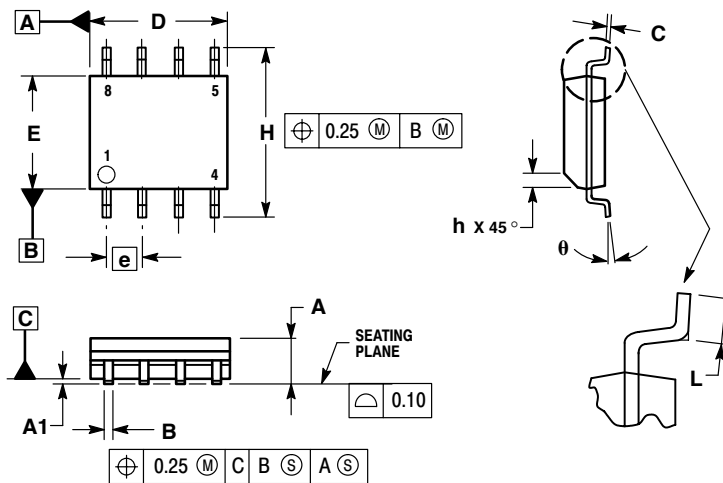


NOTES:

1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.40 | 10.16 | 0.370 | 0.400 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 3.94 | 4.45 | 0.155 | 0.175 |
| D | 0.38 | 0.51 | 0.015 | 0.020 |
| F | 1.02 | 1.78 | 0.040 | 0.070 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 0.76 | 1.27 | 0.030 | 0.050 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | --- | 10° | --- | 10° |
| N | 0.76 | 1.01 | 0.030 | 0.040 |

SO-8
D SUFFIX
CASE 751-06
ISSUE T




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.19 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BSC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.25 |
| θ | 0° | 7° |

Notes

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